REMARKS

Claims 1-6 and 9-42 will be pending in the current Application. Claims 41 and 42 have been added. Applicants submit that the amendments do not add new matter to the current Application. All the amendments herein have been made in order to clarify the claims and not for prior art reasons. Applicants also submit that (1) no amendment made was related to the statutory requirements of patentability unless expressly stated herein, and (2) no amendment made was for the purpose of narrowing the scope of any claim, unless Applicants have argued herein that such amendment was made to distinguish over a particular reference or combination of references.

Rejection of Claims 1-6 and 9-40 under 35 U.S.C. 112, second paragraph

The Examiner states that because claims 1 and 37 recites a limitation of "providing a circuit simulator having the capability of simulating changes to at least one of power supply voltage, ...", the claims are indefinite. Applicants respectfully disagree. Firstly, this element is simply defining what type of circuit simulator is to be applied to the first circuit design to derive the first set of constants for the plurality of constants. That is, the circuit simulator should be capable of simulating changes to at least one of power supply voltage, distributed capacitance, distributed resistance, transistor performance, and temperature. Secondly, the claim clearly includes how this circuit simulator is used (e.g. "applying the circuit simulator to the first circuit design...") Therefore, this language is clear and definite.

The Examiner proceeds to state that "it is unclear from the language of the claim whether the recited features are performed as components of the method" and that "it is unclear how the recited functions contribute to the claimed method." The steps of the method claims are clearly written and because they are part of the method claims, they are clearly "components of the method." Therefore, Applicants submit that it is improper for the Examiner to simply dilute claim 1 into the steps of "providing a first circuit design; changing the first circuit design...; and making an integrated circuit." The Examiner states that "none of the other recited steps contribute to the stated purpose of the preamble." However, this is incorrect. Firstly, the preamble is not limiting. Secondly, there can be numerous steps in making an integrated circuit,

including steps related to the design phase, layout phase, processing phase, manufacturing phase, etc., where any of these steps can be included in method claims for making an integrated circuit. The elements stated in claim 1 are clearly related to the result of "making an integrated circuit comprising the second circuit design." That is, as recited in claim 1, an equation must be provided, a first set of constants derived, using the first set of constants to obtain a performance model, and performing a first set of timing analyses using the performance model of the first circuit design. These steps are required with respect to the first circuit design, and clearly contribute to the claimed method. Simply because the first circuit design can be changed to a second circuit design which is included in the integrated circuit does not mean that any steps related to the first circuit design do not contribute to the overall method. Furthermore, each of the steps is clearly described in the specification as to how they are related to making an integrated circuit (see, e.g., FIG. 8; see also pages 25 – 26 to see how the steps of the method of claim 1 can fit into the process of making an integrated circuit). As described by the specification, each step of claim 1 and claim 37 does contribute to the method. Therefore, for at least these reasons, Applicants submit that claims 1 and 37 are patentable under 35 U.S.C. 112.

With respect to claim 2, Applicants agree with Examiner that claim 2 recites additional steps of claim 1 and that these steps would be optional. That is, any dependent claim can be considered as "optional" since they add optional elements to the independent claim. The Examiner states that "claim 1 has achieved the stated purpose of the preamble" and that therefore "the steps of claim 2 would fail to contribute to the method, which has been fulfilled by claim 1, and these steps would be, at best, optional." The Examiner, for this reason, states that claim 2 is vague and indefinite. However, under the Examiner's logic, any dependent claim in any existing patent would be invalidated. Furthermore, the Examiner indicates that the steps of claim 2 are "apparently to be performed after the completion of claim 1." However, note that these steps appearing in a dependent claim do not imply order, and may be performed anywhere within the method of claim 1 and do not necessarily have to be performed after completion of claim 1. Therefore, for at least these reasons, Applicants submit that claim 2 is also patentable under 35 U.S.C. 112.

With respect to claim 3, the Examiner states that recitation of the term "related" is so broad that "it is unclear what is properly excluded from the language of this claim" and proceeds to conclude that "the language fails to particularly point out and distinctly claim the invention."

However, even though the term "related" can be broadly interpreted, it does not make the claim indefinite under 35 U.S.C. 112. Furthermore, the metes and bounds of what is being claimed is clear, where the variables of the equations are described through the specification, such as throughout pages 6-21. Furthermore, there can be other aspects of an integrated circuit that are not related to the parameters provided in claim 3; therefore, the Examiner cannot simply say that the claim would be anticipated by any variable "related to an integrated circuit." At a minimum, the variables have to be related to power supply voltage, metallization capacitance, metallization resistance, transistor performance, and temperature. Therefore, although the language of claim 3 may be broad, Applicants submit that claim 3 is still definite and therefore patentable under 35 U.S.C. 112.

In addressing claims 4, 13, and 25, the Examiner states that the steps of claim 1 are "not indefinite per se" and "may not be improper under 35 U.S.C. 112". Applicants do agree with this. The Examiner proceeds to state, though, that the steps of claim 1, while not indefinite per se, contains "no positive recitation of how to 'provide an equation', what is literally involved in 'obtaining a performance model', what type of timing analyses are performed, or how the timing analyses use the performance model." However, note that each of these steps is clearly described in the Specification and would clearly be understood by those of ordinary skill in the art (e.g., pages 6-21 describes the equations in detail and pages 21-26 provide an example of how the equation is used in designing and making an integrated circuit). No extra recitations are needed to make the claim clear. Furthermore, Applicants chose not to include additional details in the claim, since only those elements currently recited in claim 1 are sufficient to make the claim novel and non-obvious over the cited art. In concluding, the Examiner states that "these recitations in claim 1 may not be improper under 35 U.S.C. 112, however they create difficulties regarding claims 4, 13, and 25." Applicants agree that the recitations in claim 1 are NOT improper under 35 U.S.C. 112. However, Applicants disagree that they create difficulties regarding claims 4, 13, and 25.

The Examiner, with respect to claims 4, 13, and 25, state that these claims "do not further limit the method of claim 1." The Examiner proceeds to state that "because claim 1 vaguely and broadly recites the use of the equation, the additional structure recited in claims 4, 13, and 25 have no direct relation to the method steps of claim 1." However, Applicants respectfully disagree. Each of these claims further limits the method of claim 1 by further defining the

equation which is applied. The Examiner states that "the inclusion of, for example 'delay expressions' in the equation of claim 1 does nothing to limit the method defined by claim 1 because there exists no positive recitation in claim 1 of how the method depends upon, uses, manipulates, or recognizes 'delay expressions' in the equation." Applicants disagree. Firstly, the equation is clearly used in claim 1, where the equation, in the embodiment of dependent claim 4, has to further include a delay expression. That is, for the embodiment of dependent claim 4, not just any equation can be used, but it has to be one that at least includes a delay expression (which are described, for example, in pages 6-12 of the Specification). Of course claim 1 does not include a positive recitation of how the method uses "delay expressions" because the detail of "delay expressions" is not even introduced until dependent claim 4. Also, the method of claim 4 is not functionally equivalent to the method of claim 1, as asserted by the Examiner, because in claim 1, the equation that is provided and used within the method need not include the delay expressions of claim 4. That is, a method in which an equation is provided that does not have to have delay expressions is not necessarily functionally equivalent to a method in which an equation is provided that requires delay expressions. Similarly, claim 13 requires an equation which comprises at least one capacitance expression, which is not required by claim 1, and these are described, for example, in the Specification on pages 12-14. Similarly, claim 25 requires an equation which comprises at least one setup/hold time expression, which is not required by claim 1, and are described, for example, in the Specification on pages 14-17. Therefore, each of claims 4, 13, and 25 further narrow claim 1 by further defining what is necessary in the provided equation and their metes and bounds are clearly described in the Specification, and for at least these reasons, Applicants submit that claims 4, 13, and 25 are patentable over 35 U.S.C. 112.

Dependent claims 5-12, 14-24, 26-35, and 40 are also allowable since they depend directly or indirectly from allowable claims 4, 13, or 25.

With respect to claims 36 and 38-39, the claims are allowable for the same reasons discussed above with respect to claim 3. That is, the use of the broad term "related" does not render the claims indefinite.

Rejection of Claims 1-6, 7-35, and 37-40 under 35 U.S.C. 112, first paragraph

The Examiner states that claims 1-6, 7-35, and 37-40 are rejected under 35 U.S.C., first paragraph, because the claims contain subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventors, at the time the application was filed, had possession of the claimed invention. However, Applicants strongly disagree. For example, each of the delay, capacitance and setup/hold time equations are fully described in pages 6-21, and a method of using these equations to make an integrated circuit is described on pages 21-27, with respect to, e.g., FIG. 8. This text clearly supports each of the claims. Therefore, the claims are clearly patentable under 35 U.S.C. 112.

The Examiner states that "the numerous difficulties under 35 U.S.C. 112, second paragraph, set forth above, necessitate this rejection of the claims under 35 U.S.C. 112, first paragraph." As pointed out in the above discussions, Applicants submit that there are no difficulties present under 35 U.S.C. 112, second paragraph. The Examiner further states that "the claims as drafted are drawn to an invention that is not disclosed in the specification." However, this is incorrect. The claims are clearly described throughout the specification. For example, see pages 21-27, which describe FIG. 8. Furthermore, Applicants disagree with the Examiner that the claims "fail to require several critical steps." The Specification does not indicate any particular step or element as critical or essential, and thus, the claims do not fail to include critical steps.

Claim Interpretation and Rejection of Claims 1-6 and 9-40 under 103(a)

Firstly, the Examiner states that "because of the 35 U.S.C. 112, first and second paragraph rejections, the claims are so indefinite and incomplete that no art rejection would be warranted, as substantial guesswork would be involved in determining the scope and content of these claims," and that "it is essentially unknown what the metes and bounds of the claims are." However, Applicants respectfully disagree with these statements. The drafted claims are all definite and clearly supported by the Specification. And although the Examiner may assert an art

rejection in view of the broadest and most reasonable interpretation of the claims, the Examiner still has to be reasonable in his interpretation and address all claim elements.

Secondly, Applicants wish to point out that the pertinence of the cited prior art reference with respect to the rejection of the independent claims and their respective dependent claims is not apparent and, further, that the rejection of the claims is not clearly explained as per the requirements outlined in 37 C.F.R. 1.104(c)(2). Applicants also respectfully points out to the Examiner that "[a] plurality of claims should never be grouped together in a common rejection, unless the rejection is equally applicable to all claims in the group" (MPEP 707.07(d)). In the current rejection, the Examiner does not address each and every element of claims 1 and 37, and does not address any of the dependent claims, which all include elements which differ from those of the independent claims.

Applicants respectfully submit that claims 1-6 and 9-40 are patentable under 35 U.S.C. 103(a). In rejecting the claims over Chang, the Examiner incorrectly ignores elements which appear in claims 1 and 37. For example, claim 1 specifically claims providing an equation which comprises a plurality of variables and constants, where the plurality of constants are unknown constants and one of the variables is related to at least one of metallization capacitance and metallization resistance; applying the circuit simulator to a first circuit design to derive a first set of constants for the plurality of constants; replacing the unknown constants with the first set of constants to obtain a performance model of the first circuit design; and performing a first set of timing analyses using the performance model of the first circuit design. These elements clearly appear in the claim and contribute to the method; however they were not specifically addressed in rejecting the claims over Chang. The Examiner simply makes broad statements with respect to his claim interpretations.

For example, simply because Chang may teach the influence of metallization resistance and metallization capacitance on IC performance does not mean Chang teaches or suggests each and every element of the claims, as required to make a proper prima facie showing under 35 U.S.C. 103. Similarly, the Examiner states that "Change teaches variables that are related to metallization resistance and metallization capacitance," and then states that "Chang discloses numerous equations used to model the performance of the IC design" and simply cites the majority of the patent which lists equations. However, there is no teaching or suggestion of providing the equation as claimed, applying the circuit simulator to obtain a first set of constants,

replacing the unknown constants with the first set of constants to obtain a performance model, and performing a first set of timing analyses using this performance model. Therefore, for at least these reasons, Applicants submit that the pending claims are patentable over Chang.

Conclusion

The Office Action contains numerous statements characterizing the claims, the Specification, and the prior art. Regardless of whether such statements are addressed by Applicant, Applicant refuses to subscribe to any of these statements, unless expressly indicated by Applicant.

Applicants respectfully solicit allowance of the pending claims. Contact me if there are any issues regarding this communication or the current Application.

If Applicant has overlooked any additional fees, or if any overpayment has been made, the Commissioner is hereby authorized to credit or debit Deposit Account 503079, Freescale Semiconductor, Inc.

Respectfully submitted,

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